

## ABSTRACT OF THE DISCLOSURE

Disclosed is an electrical device having, and a process for forming, a shallow junction with a variable concentration profile gradation of dopants. The process of the present invention includes first providing and masking a surface on an in-process integrated circuit wafer on which the shallow junction is to be formed. Next, a low ion velocity and low energy ion bombardment plasma doping or PLAD operation is conducted to provide a highly doped inner portion of a shallow junction. In a further step, a higher ion velocity and energy conventional ion bombardment implantation doping operation is conducted using a medium power implanter to extend the shallow junction boundaries with a lightly doped outer portion. In various embodiments the doping steps can be performed in reverse order. In addition, an anneal step can be performed after any doping operation.

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